Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.An auto-recovery wafer testing method, comprising:
a first testing step to test sequentially a plurality of chips on a wafer and spontaneously save testing data for each of the chips;
an auto-recovery data generating step, wherein, if the first testing step is accidentally interrupted, auto-recovery data are generated based on the testing data that is saved; and
a second testing step for continuing the testing, based on the auto-recovery data, from a chip being last but incompletely tested.

[c2] 2. The wafer testing method as recited in claim 1, wherein, during the first testing step, a first testing unit is used to test the chips and output corresponding testing data for each of the chips.

[c3] 3. The wafer testing method as recited in claim 1, wherein, during the first testing step, a real-time accessing module is used to instantaneously save testing data for each of the chips.

[c4] 4. The wafer testing method as recited in claim 1, further

comprising a problem-eliminating step, after the auto-recovery data generating step and before the second testing step, so as to ensure the first testing unit operating properly.

[c5] 5. The wafer testing method as recited in claim 4, wherein, during the second testing step, the first testing unit is used for continuing the testing, based on the auto-recovery data, from a chip being last but incompletely tested.

[c6] 6. The wafer testing method as recited in claim 1, further comprising a transfer step, after the auto-recovery data generating step and before the second testing step, so as to transfer the wafer from the first testing unit to a second testing unit.

[c7] 7. The wafer testing method as recited in claim 6, during the second testing step, the second testing unit is used for continuing the testing, based on the auto-recovery data, from a chip being last but incompletely tested.

[c8] 8. An auto-recovery wafer testing apparatus suitable for testing a plurality of chips on a wafer, comprising:
a main system used to control overall wafer testing process;
a tester, electronically coupled to the main system and

used for receiving commands from the main system, testing the chips sequentially, and output a plurality of corresponding testing data; and

a real-time accessing module, electronically coupled to the tester and used for saving instantaneously the testing data, wherein, if the testing is accidentally interrupted, the tester generates auto-recovery data based on the testing data saved in the real-time accessing module, and continues the testing, based on the auto-recovery data, from a chip being last but incompletely tested.

[c9] 9. The wafer testing apparatus as recited in claim 8, wherein the tester comprises:

a testing unit; and

a control module, electronically coupled to the main system, the real-time accessing module and the tester, wherein, the control module receives commands from the main system to control the testing of the testing unit and output the testing data to the real-time accessing module, and if the testing is accidentally interrupted, the control module generates the auto-recovery data, based on the testing data saved in the real-time accessing module, for controlling the testing unit to resume the interrupted testing.

[c10] 10. The wafer testing apparatus as recited in claim 9, wherein the testing unit comprises a prober.

[c11] 11. The wafer testing apparatus as recited in claim 9, wherein the testing unit comprises a laser trimmer.